In the Specification

Please amend the specification of this application as follows:

Insert the following after page 8, line 7:

--SUMMARY OF THE INVENTION

A method of exporting emulation information from a data processor and an integrated circuit and data processing system that can practice the method. The method collects internal emulation information at a data processor clock rate, arranging the emulation information into first information blocks of a first fixed size. The method arranges the emulation information into second information blocks having a different second fixed size. The method outputs the second information blocks at a transmission clock rate. An external system receives the second information blocks and re-arranges the second information blocks into first information blocks.

The respective first and second fixed sizes, the data processor clock rate and the transmission clock rate are related so that bit rate of first information blocks equals the bit rate of second information blocks. When the second fixed size is smaller than the first fixed size, then the transmission clock rate is greater than the data processor clock rate. When the second fixed size is larger than the first fixed size, the transmission clock rate is less than the data processor clock rate.

When the first fixed size is an integral multiple of the second fixed size, first information blocks are stored in a current first information block in a current packet register. Second information blocks are sequentially extracted from the current packet register. Once all bits in the current packet register are selected, a next first information block is stored in the current packet register and the process repeats.

When the first fixed size is not an integral multiple of said second fixed size, first information blocks are stored in a current packet register and a last packet register. Second information blocks are selected from the current packet register until a number of bits of remaining in the current packet register is less than the second fixed number. The current first information block is store in the last packet register and a next first information block is stored in the current packet register. Then second information blocks are selected bits remaining in the last packet register and bits starting at a first bit of the current packet register. This process repeats when the first information block in the current packet register is completely selected. There are three alternatives if no valid first information block is available. The selection and output of second information blocks could stall immediately. The selection and output of second information blocks could continue until all first information blocks are output, including NOP bits in the last second information block if needed, and thereafter stall. The selection and output of second information blocks could continue with NOP bits following the last valid first information block.--